

Form PTO-1449 LIST OF PRIOR ART CITED BY APPLICANT <i>(Use several sheets if necessary)</i>	ATTORNEY DOCKET NO. YOR920030387US1	SERIAL NO. Not Assigned <i>10/696, 139</i>
	APPLICANT Rhee et al.	
	FILING DATE October 29, 2003	GROUP ART UNIT Not Assigned <i>2816</i>

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO	

OTHER PRIOR ART (including author, title, date, pertinent page, etc.)

<i>und</i>	AA	Sidiropoulos et al., "A Semidigital Dual Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1683-1692.

RELATED PATENT APPLICATIONS

EXAMINER INITIAL	APPLICATION NO/ ATTY. DOCKET NO.	APPLICANT	TITLE	FILING DATE

DATE CONSIDERED <i>Nov 2, 2004</i>	EXAMINER <i>[Signature]</i>
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